CLAIMS

We Claim:

1. In a semiconductor device having at least an insulating gate dielectric layer and a gate fabricated upon a semiconductor substrate, a buried channel implanted below the insulating gate dielectric layer, the buried channel being doped with a predetermined dopant so that when the gate is biased with respect to the substrate, the buried channel is partially depleted of charge carriers, effectively increasing the thickness of the insulating gate dielectric layer.

2. The device of claim 1 wherein the substrate is a p-type substrate and the buried channel is an n-type buried channel.

3. The device of claim 1 wherein the substrate is an n-type substrate and the buried channel is a p-type channel.

4. The device of claim 2 wherein the bias from the gate to the substrate is an inversion bias.

5. The device of claim 3 wherein the bias from the gate to the substrate is an inversion bias.

6. The device of claim 1 wherein the device is an NMOS transistor.

7. The device of claim 1 wherein the device is a PMOS transistor.

8. The device of claim 1 wherein the device is a MOS capacitor.

9. The device of claim 8 wherein the MOS capacitors comprise part of a one transistor random access memory.

10. In an integrated circuit fabricated on a semiconductor substrate, the integrated circuit comprised of a plurality of devices, at least one of the devices having a gate and an insulating dielectric layer between the gate and the substrate, a method for increasing the effective thickness of the dielectric layer, the method comprising the step of implanting a buried channel between the substrate and the dielectric layer, the buried channel being

doped so that when the device is operating at a predefined bias voltage, the buried channel is partially depleted of charge carriers, the depleted buried channel thereby adding to the effective thickness of the adjacent dielectric layer.

11. The method of claim 10 wherein the integrated circuit comprises a plurality of PMOS and NMOS devices, wherein each such NMOS and PMOS device has at least a first substrate type, a gate and a dielectric layer separating the gate from the substrate, and wherein each device has a buried channel of a second and opposite type from the substrate type.

12. A method of increasing the effective thickness of an oxide layer in a semiconductor device, the method comprising the step of implanting a region between the oxide layer and a substrate layer upon which the oxide layer is grown, the region becoming partially depleted of charge carriers when the device is operating with a predefined bias voltage, the region thereby effectively increasing the thickness of the oxide layer.

13. The method of claim 12 wherein the substrate layer is a p-type substrate layer and the region is an n-type region.

14. The method of claim 12 wherein the substrate layer is a n-type substrate layer and the region is a p-type region.

15. An integrated circuit fabricated with a plurality of semiconductor devices, the devices being fabricated according to the method of claim 12.

16. The integrated circuit of claim 15 wherein at least a plurality of the semiconductor devices comprise a gate, a gate dielectric and a substrate, each of the plurality additionally having a region between the gate dielectric and the substrate.

17. The integrated circuit of claim16 wherein the semiconductor devices have either a p-type or an n-type substrate and the region may be either p-type or n-type, except that the substrate and the region of each device having a region must be of different type.

18. The integrated circuit of claim 17 wherein at least one of the devices is an NMOS transistor.

19. The integrated circuit of claim 17 wherein at least one of the devices is a PMOS transistor.

20. The integrated circuit of claim 17 wherein at least one of the devices is an MOS capacitor.

21. The integrated circuit of claim 20 wherein at least one MOS capacitor comprises part of a one transistor random access memory.